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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – FAT

Course Code: ECE1003 | **Course Title: Digital Logic design**

Set number: 14 | **Date of Exam:** 16/06/2023 (FN) (A1)

Duration: 120 | **Total Marks: 60**

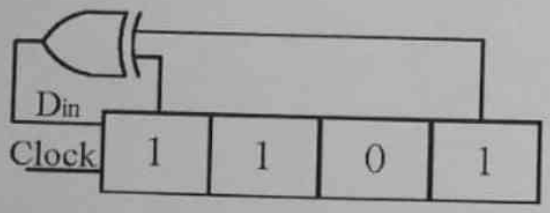
Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

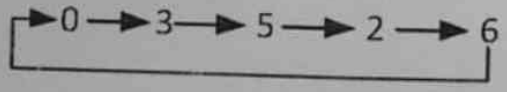
Q1. Realise the following Boolean function using: a) 8X1 b) 4X1 Multiplexer.

$F(A, B, C, D) = \sum m(0, 2, 3, 5, 8, 10, 11, 12, 15)$ **(10M)**

Q2. A 4-bit shift register, which shifts one bit to the right at every clock pulse, is initialized to values "1101". as shown below. How many clock pulses are needed for pattern "1111" and write down the logic table? **(10M)**



Q3. Design a synchronous counter of the following sequence using J-K flip-flop **(15M)**



Q4. Implement the Boolean functions F1 = A'BC'D + A'BCD' + ABC'D and F2 = A'BC' + A'BC + AB'C + ABC' with PAL device. **(15M)**

Q5. Implement the following Boolean function using CMOS logic **(10M)**

$$Y = (A + B)(C + D)$$

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023–FAT

Course Code: ECE1003

Course Title: Digital Logic Design

Set number: 6

Date of Exam: 16/06/2023 (AN) (A2)

Duration: 120 mins

Total Marks: 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Design a synchronous sequential circuit to obtain the sequence 1,3,2,0 using minimum number of T flip flops. **(15M)**

Q2. Design the internal logic diagram of a PLA to implement the functions $F1 = \bar{A}B + A\bar{C} + ABC + B\bar{C}$ and $F2 = \overline{\bar{A}B + A\bar{C} + \bar{A}\,\bar{B}}$. **(15M)**

Q3. Design a decoder circuit to obtain the following Boolean functions $F1(a,b,c,d) = \sum(9,11,13,15)$, $F2 = \sum(0,1,3,4,5)$ (use only 1 decoder with appropriate number of input and output). **(10M)**

Q4. *Implement JK flip flop using T flip-flops and appropriate logic gates.* **(10M)**

Q5. *Implement the logic function* $F = \overline{\bar{A}B + AC}$ *using CMOS logic. If ABC=110 what will be the state of each transistor in the designed circuit and obtain the output for the given value of ABC. Include appropriate NOT implementations for obtain complement terms.* **(10M)**

QP MAPPING

lo.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
	3	3	1,2,3,4,6	1,2	1,2	15
2	4	4	1,2,3,4	1,2	1,2	15
3	2	2	1,2,3,4,10	1,2	1,2	10
4	3	3	1,2,3,4,6	1,2	1,2	10
5	5	5	1,2,3,4	1,2,3	1,2	10

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QUESTION PAPER

Name of the Examination: WIN 2022-2023 – FAT

Course Code: ECE1003 **Course Title:** Digital Logic Design

Set number: 03 **Date of Exam:** 17/6/2023 (FN) (B1)

Duration: 120 min **Total Marks:** 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Implement this function: $F(A,B,C) = \sum(0,2,3,4)$ using only 2*4 decoders. **(10M)**

Q2. How can a T flip-flop be converted into a JK flip-flop? **(10M)**

Q3 Design a 4-bit synchronous counter using negative edge-triggered T flip-flops that goes through the sequence 0, 2, 3, 5, 7, 11, 13, 0. **(15M)**

Q4. Design PLA realization of full adder. **(15M)**

Q5. Design a CMOS Logic Circuit for 2 input XOR gate. **(10M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1,2	2	1	10
Q2	3	3	1,2	2	1	10
Q3	3	3	1,2	2	1	15
Q4	4	4	1,2	2	1	15
Q5	5	5	1,2	2	1	10

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – FAT

Course Code: ECE1003

Course Title: Digital Logic Design

Set number: 11

Date of Exam: 19/06/202

Duration: 120 mins

Total Marks: 60

(C1)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable. **(10M)**

Q2. Convert S-R flip-flop to D flip-flop? **(10M)**

Q3. Design a 3-bit synchronous up counter using T flip flop? **(15M)**

Q4. The following is a truth table of a three-input, four-output combinational circuit.

Tabulate the PAL programming table and draw the PAL circuit diagram **(15M)**

Inputs			Outputs			
x	*y*	*z*	*A*	*B*	*C*	*D*
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	1	0	1	0	1	0
1	1	1	0	1	1	1

Q5. Implement the following Boolean function using CMOS **(10M)**

$$F = \overline{XYZ + TV + WU}$$

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – FAT

Course Code: ECE1003 | Course Title: Digital Logic Design

Set number: 8 | Date of Exam: 19/06/2023 (AN)

Duration: 120 mins | Total Marks: 60 (C2)

Instructions:

i. Assume data wherever necessary.

ii. Any assumptions made should be clearly stated.

1. Minimize the following Boolean function using K-Maps

$$F(A, B, C) = \Sigma m(1, 2, 5, 7) + \Sigma d(0, 4, 6)$$ (10M)

2. What would be the serial output of a serial-in serial-out shift register loaded with the serial data **1010**, after 3 clock pulses? (10M)

3. Design a 4-bit synchronous counter using T flip-flops to count in the sequence from 0 to 15? (15M)

4. What Implement the following Boolean function using PROM (15M)

$F0(A,B,C) = \Sigma(1,6,7)$

$F1(A,B,C) = \Sigma(1,3,4)$

$F2(A,B,C) = \Sigma(2,5,6)$

5. Implement the CMOS logic circuit for a Boolean function $\overline{(AD + BC)}$ through its circuit diagram. (10M)

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1,2	2	1	10
Q2	3	3	1,2	2	1	10
Q3	3	3	1,2	2	1	15
Q4	4	4	1,2	2	1	15
Q5	5	5	1,2	2	1	10

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QUESTION PAPER

Name of the Examination: WIN 2022-2023 – FAT

Course Code: ECE1003 **Course Title: Digital Logic Design**

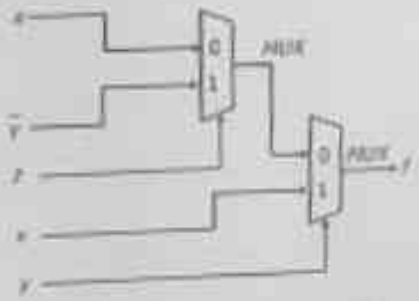
Set number: 9 **Date of Exam: 20/06/2023 (FN) (D1)**

Duration: 120 Min **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Consider two 2-to-1 multiplexers given below. Find the sum-of-products form of the Boolean expression for the output (f) of the multiplexer. **(10 M)**



Q2. Initial content of a 4-bit serial-in parallel-out (right) sift register with the combinational circuit arrangement is 1010. How many clock pulses will be required to repeat the same content in the register. **(10 M)**

Q3. Design a 3-bit synchronous up counter using T Flipflop, which count the sequence in odd numbers (1, 3, 5, 7, 1,....). **(15 M)**

Q4. Implement the circuits using PROM and PAL for the given following expressions. **(15 M)**

$F_1(A, B, C) = \sum(0, 1, 6, 7)$ & $F_2(A, B, C) = A'B + AC'$

Q5. Implement the following Boolean expression with minimum number of CMOS transistors. You can assume both the original and complemented versions of each literal are available as gate inputs. **(10 M)**

$$(A'.B + A.C').D$$